Remarks

Entry therefor of this Supplementing Amendment prior to the Examiner taking up the responsive Amendment filed on September 3, 2002 for a formal review is respectfully requested.

The revisions being made to the Specification are to correct discovered informalities therein, including correcting also typographical errors made during the earlier preparation of the Substitute Specification, as well as to effect minor editorial clarifications. Since the revisions being made therein are strictly of a minor formal nature, acceptance and entry therefor of the same is respectfully requested.

Turning to the claims, independent claim 3 is being further amended to achieve description consistency of the expressions employed in the body of that claim. Specifically, the expression "said insulating film" is being revised to the expression "said <u>first</u> insulating film," consistent with that it is intended to refer to. Regarding the "solution" used in the cleaning process as it relates to original dependent claims 15 and 41, as previously amended, as well as with regard to the previously newly added claims 51 and 52, an additional component, in an alternative sense, is being added thereto, in keeping with that encompassed by the originally submitted disclosure. For example, as described on page 40, at the end of paragraph [0167], as well as on page 41, paragraph [0171], for example, the cleaning solution employed contains at least one of hydrogen fluoride (HF), citric acid, oxalic acid, hydrogen peroxide (H_2O_2), hydrochloric acid (HCl), sulfuric acid (H_2SO_4), ammonia (NH_3) and <u>aminoethanol</u>. Accordingly, in order to maintain a consistency with that afforded by the original disclosure, the just noted claims have been amended, accordingly.

Multiple dependent claims 6 and 7 are being amended, furthermore, so as to more appropriately conform to the requirements concerning the drafting of dependent claims,

whether they are in single claim dependency format or in a multiple claim dependency format. Specifically, claim 6 as well as claim 7 were amended so as to remove the additional reference to more than one claim in the body of those claims. In this connection, the present amendments made to multiple dependent claim 6, in conjunction with the newly added claim 55, cover all of the alternative combinations previously existing in multiple dependent claim 6. Likewise, the present amendments made to multiple dependent claim 7, in conjunction with the newly added dependent claims 56 and 57, cover the various alternative possibilities previously covered by multiple dependent claim 7. Since these changes are strictly of an editorially clarifying nature and are also in keeping with the statutory and rule requirements regarding the drafting of dependent claims, acceptance and formal entry therefor of the same is respectfully requested. It is also noted that the submission of claims 55-57 should not result in an additional claim fee since they are, basically, individual sub-components of previously pending claims 6 and 7.

A marked-up copy showing changes made is included as Attachment A.

Favorable action therefor of all of the presently pending claims, i.e., claims 1-17, 37 and 39-57, for the reasons noted in the earlier submitted response, filed on September 3, 2002, and as supplemented hereinabove, as well as an early formal notification of allowability of the above-identified application are respectfully requested.

Concurrently filed herewith, also, is an Information Disclosure Statement (IDS) including copies and a listing therefor of documents uncovered by applicants, in keeping with the duty of disclosure/candor requirements. These art documents disclose wiring/interconnection manufacturing schemes. The following discussion is directed, it is believed, to the two most pertinent ones of the listed art documents to the present claimed subject matter. As is shown hereinbelow, however, the present claimed subject matter is

considered to be defining thereover.

I. <u>Maeda (JP 11-016906 A)</u>

Maeda's disclosure is particularly directed to the manufacture of a cap layer (e.g., tungsten [W] layer 11b) which is formed to be in self-alignment with the wiring layer (e.g., Cu layer 4), by the CVD method (see Fig. 3 in Maeda). In accordance with Maeda's manufacturing scheme associated with the formation of cap layer on the wiring layer, the following process steps are employed:

forming the insulator film 1;

forming the interconnect groove 2 and a through-hole 6 in the insulator film 1 by the PR or RIE method;

forming the barrier metal layer 3 in the interconnect groove 2 and in the through-hole 6;

forming the wiring layer 4 on the barrier metal 3, completely filling the interconnect groove 2 as well as the through-hole 6;

removing both the metal barrier layer 3 and the wiring layer (Cu 4) from outside of the interconnect groove 2 by a polishing process (CMP);

and, followed by the formation of the cap layer 11b on the wiring layer 4 by selective growth using the CVD method.

It is noted, however, that Maeda's manufacturing scheme does not include at least the steps of performing a treatment of the surface of the wiring layer 4 and that of the insulator film 1 subsequent to the polishing step performed by the CMP method as well as after the formation of the cap layer 11b, in clear contradistinction with that called for by the present claimed subject matter. An example of such treatments which are not taught by Maeda include at least step (c) in claim 1, and also that featured in claim 17, etc. Such featured aspects, among other aspects of the method for manufacturing the semiconductor integrated circuit device presently called for, are also found in other ones of the presently pending claims.

II. <u>Tobben et al (US 6,261,950 B1)</u>

Tobben et al's disclosure is particularly directed to the method of fabricating a self-aligned metal cap used in the interlayer wiring connections. With regard to this, the discussion in column 4, lines 1-58 as it relates to the process shown in Figs. 2-4 of Tobben et al, is directed to the method of fabricating metal cap 110 (e.g., tungsten layer) to be in self-alignment with the metal structure 114, using the CVD growth process. According to Tobben et al's scheme, the process of fabricating the self-aligned metal cap, such as metal layer 110, shown in Figs. 2-4, includes the following steps:

forming the dielectric layer 102;

forming the via 106 and the trench 108 in the dielectric layer 102 by the RIE method;

forming a conductive structure 114 by completely filling the via 106 and trench 108 with a metal (e.g., Al, Cu and alloys thereof), in which the top surface of the conductive (wiring) structure is planarized to that of the top surface 112, for example, by CMP (cleaning may be employed to strip surface 112 of any native oxide, although this may be unnecessary as noted in column 4, lines 11-14);

selectively forming metal layer 110 (e.g., tungsten layer) on the polished metal surface of structure 114 by using a selective tungsten deposition in connection with the CVD method employed (column 4, lines 14-20, in Fig. 2);

forming the interlayer dielectric 120 and forming a via 122 (see Figs. 3 and 4); and

cleaning to remove the native oxide from metal layer 110 (column 4, lines 52-58 in Fig. 4 in Tobben et al).

It is also apparent that Tobben et al's disclosure also does not teach the present claimed invention. For example, it is noted that Tobben et al's disclosure failed to teach at least a cleaning treatment on the upper surface of the dielectric layer 102 prior to the selective deposition of the cap layer (e.g., tungsten layer 110), as that presently called for in claims 1+, etc. It is noted, also, any cleaning performed according to Tobben et al's process, as noted above, is in the form of a target cleaning, namely, cleaning to remove

native oxide on the metal layer 110. It is submitted, Tobben et al neither disclosed nor suggested a problem associated with metallic contaminants on the dielectric layer 102 which may lead to the undesired growth thereof in the case of breakage of tungsten material in connection with the selective deposition of tungsten in the formation of the cap layer. Also, even the target cleaning of the native oxide may be unnecessary according to Tobben et al, as discussed above, due to the fact that the native oxide from layer 110 is removed after the step of forming the via 122 which exposes the tungsten layer 110, at that time, as shown in Fig. 4. It is clearly apparent, therefore, that Tobben et al's disclosure failed to disclose or suggest as fabrication scheme as that presently called for.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (501.39868X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
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MARKED-UP VERSION SHOWING CHANGES MADE

IN THE SUBSTITUTE SPECIFICATION:

Please amend paragraph [0064] as follows:

[0064] Subsequently, as shown in Fig. lb, the semiconductor substrate 1 is cleaned on the surface thereof by wet etching using, for example, hydrofluoric acid, and it is subsequently thermally oxidized at about 800 to 850°C to form a clean gate oxide film 5 having a thickness of approximately [7 mm] <u>7nm</u> on the surface thereof.

Please amend paragraph [0066] as follows:

[0066] Thereafter, as shown in Fig. 2b, an n-type impurity (phosphorus (P) or arsenic (As)) is ion-implanted into the semiconductor substrate 1 at opposite sides of the gate electrode 7 on the p-type well 3, thereby forming n-type semiconductor regions 8 (source, drain). Likewise, a p-type impurity (e.g. boron) is ion-implanted into the semiconductor substrate 1 at opposite sides of the gate electrode 7 on the n-type well 4, thereby forming p-type semiconductor regions <u>9</u> (source, drain).

Please amend paragraph [0076] as follows:

[0076] Next, as shown in Fig. [Sa] <u>5a</u>, a titanium nitride film (not shown) is formed, by the CVD method, on the interlayer insulating film 18 including the contact hole 20, followed by further formation of a tungsten (W) film (i.e. a first conductive film defined in Claim 3). Next, the titanium nitride film (TiN) and the tungsten film are removed by CMP from portions other than the contact hole 20. It will be noted that the

titanium nitride film may be formed by a sputtering method. The titanium nitride film may be formed of a laminated film consisting of titanium (Ti) and titanium nitride (TiN).

Please amend paragraph [0090] as follows:

[0090] Next, as shown in Fig. 8a, a silicon nitride film 28 is formed on the silicon oxide film 23 and the wiring 26 (tungsten film 26c), followed by further deposition of [asilicon oxidefilm] <u>a silicon oxide film</u> 29 by a CVD method.

Please amend paragraph [0100] as follows:

[0100] The plug 31 is formed in the following manner. Initially, after formation of a titanium nitride film [31] <u>31a</u> by a CVD method or sputtering method on the silicon oxide 29 including the inside of the contact hole 30, a tungsten film 31b is formed according to a CVD method. Next, the titanium nitride film 31a and the tungsten film 31b, both outside the contact hole 30, are removed by CMP, thereby forming the plug 31. It should be noted that, like the wiring 26, a copper film may be formed on the titanium nitride film 31a by sputtering or plating, thereby providing a copper plug 31. In this case, there may be used, in place of the titanium nitride film 31a, not only a single-layered film, for example, of tantalum, tantalum nitride, tungsten or tungsten nitride and a three-layered laminated film wherein a titanium nitride film is formed on a titanium film, on which a titanium film is further formed (Ti/TiN/Ti), but also a laminated film of Ti/TiN, Ta/TaN/Ta, Ta/TaN or the like.

Please amend paragraph [0102] as follows:

[0102] Thereafter, like the case of the wiring groove 25, the silicon oxide film 33 is removed by etching from a region where a second wiring is to be formed[,] . The silicon nitride film 32 exposed by the etching is further etched to form a groove 34 for wiring.

Please amend paragraph [0115] as follows:

[0115] In the embodiment described hereinabove, the wiring 26 is formed as a first layer wiring and the wiring 35 is formed as a second layer wiring, and the aluminum wiring 40 is formed on the second layer wiring via the plug 39. Alternatively, as shown in Fig. 12, a third layer wiring M3 and a fourth layer wiring M4 may be formed between the second layer wiring 35 and the aluminum wiring 40. In such a case, the third layer wiring M3 and the fourth layer wiring M4 may be, respectively, formed like the first and second layer wirings 26, 35 wherein tungsten films M3c, M4c are, respectively, formed on the wiring surface. A plug P3 between the third layer wiring and the fourth layer wiring and a plug P4 between the fourth layer wiring and the aluminum wiring 4 may be, respectively, formed in the same manner as the plugs 31, 39. Reference numerals 49, 51, [53] 52 and 55, respectively, indicate a silicon nitride film, and reference numerals 50, [52] 53, 54 and 56, respectively, indicate a silicon oxide film.

Please amend paragraph [0150] as follows:

[0150] Further, as described in Embodiment 1 while referring to Fig. 29,

the formation of the tungsten film 35c can prevent the surface of wiring 35 from being [oxidizing] oxidized, reducing the rise in the wiring resistance.

Please amend paragraph [0154] as follows:

[0154] In this embodiment, although the first layer wiring 26 and the second layer wiring 35 are formed, and the aluminum wiring 40 is formed on the second layer wiring 35 through the plug 39, a third layer wiring M3 and a fourth layer wiring M4 may be formed between the second layer wiring and the aluminum wiring 40 (Fig. 21), like Embodiment 1. In such a case, the third layer wiring and the fourth layer wiring are formed according to the dual damacene method, like the first and second layer wirings. More particularly, after the formation of a wiring groove and a contact hole, they are simultaneously buried to form the wirings. The wirings are formed on the surfaces thereof with tungsten films [(3Mc, 4Mc)] (M3c, M4c).

Please amend paragraph [0156] as follows:

[0156] In Embodiments 1 and 2, after the formation of the tungsten films 26c, 35c (see [Fig. 7b] Figs. 7b and 9 in Embodiment 1 and [Fig.] Figs. 15 and 19 in Embodiment 2), the silicon nitride films 28, 36 and the silicon oxide films 29, 37 are formed on the tungsten films 26c, 35c, respectively. Alternatively, as shown in Figs. 25a and [2Sb] 25b, silicon oxide films (hereinafter referred to as TEOS film) 328, 336, which are deposited according to a CVD method using tetraethoxysilane as a starting gas, are thinly formed on the tungsten films 26c, 35c, respectively, followed by further formation thereon of insulating films 329, 337 having a dielectric constant lower than the TEOS

films (i.e. a dielectric constant of 4 or below) . It will be noted that a carbon-containing silicon-based insulating film, such as a silicon carbide film, an SiCO film or the like, may be used in place of the TEOS films 328, 336. The carbon-containing silicon-based insulating film, such as SiC or SiCO, has a dielectric constant as low as $\epsilon \approx 4$ to 6, and serves as a diffusion-preventing (barrier) layer for Cu, like a silicon nitride (SiN) film.

Please amend paragraph [0161] as follows:

[0161] In Embodiments 1 to 3, after the formation of the tungsten films 26c, 35c (see [Fig. 7b] <u>Figs. 7b and 9</u> in Embodiment 1 and [Fig.] <u>Figs. 15a and</u> 19 in Embodiment 2), the silicon nitride films 28, 36 and the silicon oxide films 29, 37 are, respectively, formed on the tungsten films 26c, 35c. Instead, as shown in Figs. 26a and 26b, insulating films 428, 436, which include a silicon nitride film, a PSG film, or a carbon-containing silicon-based insulating film, such as a silicon carbide (SiC) film or a SiCO film, and which have the capability of preventing diffusion of copper, may be formed on the tungsten films 26c, 35c. Moreover, insulating films 429, 437 made of a low dielectric material having a dielectric constant lower than the insulating films 428, 436 are formed on the tungsten films 26c, 35c, respectively. The insulating films 429, 437 made of the low dielectric material include, for example, those insulating films having a dielectric constant of 4 or below, such as a TEOS film, a SiOF film, an organic coating film, and a porous silica film.

Please amend paragraph [0167] as follows:

[0167] After CMP of the copper films 26b, 36b (see Fig. 7a in

Embodiment 1 and Fig. 18b in Embodiment 2), the substrate surfaces (including the surfaces of the copper films 26b, 35b and the silicon oxide films 23, 33) are cleaned with a cleaning solution, such as a solution[,] for removing foreign matter and contaminant metals, after which tungsten films 26c, 35c are formed on the wirings 26, 35 by selective or preferential growth. Such a solution should contain at least one of hydrogen fluoride (HF), citric acid, oxalic acid, hydrogen peroxide ($H_2 0_2$), hydrochloric acid [HC_l] (HCl), sulfuric acid (H_2SO_4), ammonia (NH_3) and aminoethanol.

Please amend paragraph [0169] as follows:

[0169] Fig. 28a is a graph showing [he] the yield for wiring [short¡circuiting] short-circuiting in the cases where cleaning with a hydrogen fluoride (HF) solution is effected for treating times of 20 seconds (B) and 60 seconds (C) and in the case where no cleaning with a hydrogen fluoride solution is effected (A).

Please amend paragraph [0184] as follows:

[0184] After the selective or preferential growth of the tungsten films 26c, 35c on the surfaces of the wirings 26, 35 (see [Fig. 7b] Figs. 7b and 9 in Embodiment 1 and [Fig. 19a] Figs. 15a and 19 in Embodiment 2), the substrate surfaces (including the surfaces of the tungsten films 26c, 35c and the silicon oxide films 23, 33, and the like) are cleaned with a solution capable of removing contaminant metals and containing at least one of hydrogen fluoride (HF), hydrogen peroxide ($H_2 0_2$), citric acid and the like, as mentioned hereinbefore.

Please amend paragraph [0185] as follows:

[0185] When the substrate surfaces are cleaned with a hydrogen fluoride (HF) solution or the like after the selective or preferential growth of the tungsten films 26c, 35c, a tungsten [.]film is grown on the silicon oxide film (i.e. breakage of the selectivity occurs) as shown in Fig. 27a. If a tungsten film is grown on a contaminant metal on the silicon oxide film as described with reference to Embodiment 5, the unnecessary tungsten film and contaminant metal are etched, thereby providing a highly reliable tungsten film.

<u>IN THE CLAIMS:</u>

Please **amend**, furthermore, claims 3, 6, 7, 15, 41, 51 and 52, as follows:

3. (Twice Amended) A method for manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) forming a first wiring on a semiconductor substrate;

(b) forming a first insulating film on said first wiring;

(c) removing said first insulating film at a portion thereof corresponding to a contact region of said first wiring to form a contact hole;

(d) forming a first conductive film over said <u>first</u> insulating film including the inside of said contact hole;

(e) removing said first conductive film from outside of said contact hole to form a plug;

(f) forming a second insulating film over said first insulating film and said plug;

(g) removing said second insulating film at a portion thereof corresponding to a region where a second wiring is to be formed, thereby forming a groove for wiring;

(h) successively forming a barrier layer and a second conductive film on said second insulating film including the inside of the said groove for wiring;

(i) removing said barrier layer and said second conductive film from outside of said groove for wiring by polishing to form a second wiring;

(j) cleaning a surface of said second insulating film to remove said second conductive film that remains on said second insulating film in said step (i);

(k) forming a cap conductive film on said second wiring in self-alignment with said second wiring by selective growth or preferential growth of said cap conductive film on said second wiring; and

(l) forming a third insulating film over said cap conductive film and said second insulating film.

6. (Twice Amended) A method for manufacturing a semiconductor integrated circuit device according to Claim [1,] 4 or 5 further comprising the steps of:

partly removing [said second insulating film defined in Claim 1,] said third insulating film [defined in Claim 4 or said third insulating film defined in Claim 5] to form an opening so that said cap conductive film is exposed;

burying a conductive material in said opening to form a plug; and

forming an upper wiring, which extends on said plug, on [said second insulating film defined in Claim 1,] said third insulating film [defined in Claim 4 or said third insulating film defined in Claim 5].

7. (Twice Amended) A method for manufacturing a semiconductor integrated circuit device according to Claim [1, 2,] 3, 4 or 5, wherein [said wiring defined in Claim 1 or] said second wiring [defined in any one of Claims 2 to 5] is made of copper, silver, aluminum or an alloy containing these metals as a main component.

15. (Twice Amended) A method for manufacturing a semiconductor integrated circuit device according to Claim 1, wherein said cleaning in said step (c) is performed by using a solution containing at least one of hydrogen fluoride (HF), citric acid, oxalic acid, hydrogen peroxide (H_2O_2), hydrochloric acid (HCl), sulfuric acid (H_4SO_4), [and] ammonia (NH_3) and aminoethanol.

41. (Twice Amended) A method for manufacturing a semiconductor integrated circuit device according to Claim 39,wherein said cleaning in said step (d) is a cleaning with a solution containing at least one of hydrogen fluoride (HF), citric acid, oxalic acid, hydrogen peroxide (H_2O_2), hydrochloric acid (HCl), sulfuric acid, [and] ammonia (NH_3) and aminoethanol.

51. (Amended) A method for manufacturing semiconductor integrated circuit device according to claim 4, said cleaning in said step (g) is performed by using a solution containing at least one of hydrogen fluoride (HF), citric acid, oxalic acid, hydrogen peroxide (H_2O_2), hydrochloric acid (HCl), sulfuric acid (H_4SO_4), [and] ammonia (NH_3) and aminoethanol.

52. (Amended) A method for manufacturing semiconductor integrated circuit device according to claim 5, said cleaning in said step (g) is performed by using a

solution containing at least one of hydrogen fluoride (HF), citric acid, oxalic acid, hydrogen peroxide (H_2O_2), hydrochloric acid (HCl), sulfuric acid (H_4SO_4), [and] ammonia (NH_3) and aminoethanol.